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BrainFrame: A node-level heterogeneous accelerator platform for neuron simulations

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December 2016

Abstract. *Objective:* The advent of High-Performance Computing (HPC) in recent years has led to its increasing use in brain study through computational models. The scale and complexity of such models are constantly increasing, leading to challenging computational requirements. Even though modern HPC platforms can often deal with such challenges, the vast diversity of the modeling field does not permit for a single acceleration (or homogeneous) platform to effectively address the complete array of modeling requirements. *Approach:* In this paper we propose and build BrainFrame, a heterogeneous acceleration platform, incorporating three distinct acceleration technologies, a Dataflow Engine, a Xeon Phi and a GP-GPU. The PyNN framework is also integrated into the platform. As a challenging proof of concept, we analyze the performance of BrainFrame on different instances of a state-of-the-art neuron model, representing the Inferior-Olivary Nucleus using a biophysically-meaningful, extended Hodgkin-Huxley representation. The model instances take into account not only the neuronal-network dimensions but also different network-connectivity circumstances that can drastically change HPC workload characteristics. *Main results:* The combined use of HPC fabrics demonstrated that BrainFrame is better able to cope with the modeling diversity encountered. Our performance analysis shows clearly that the model directly affects performance and all three technologies are required to cope with all the model use cases. *Significance:* The BrainFrame framework is designed to transparently configure and select the appropriate back-end accelerator technology for use per simulation run. The PyNN integration provides a familiar bridge to the vast array of modeling work already conducted. Additionally it gives a clear roadmap for extending the platform support beyond the proof-of-concept, with improved usability and directly useful features to computational-neuroscience community, paving the way for wider adoption.

1. Introduction

Through the efforts of biologists and computational neuroscientists in recent decades, advance models of cortical neurons were developed using Spiking Neural Networks (SNNs) [1]. These models do not just abstractly mirror aspects of biological processes, like Artificial Neural Networks (ANNs), but directly emulate them. The more complex information encoding in SNNs ensures that they have greater computational capacity [2, 3] than ANNs and allow computational scientists to begin making biologically accurate models of brain subsystems, furthering their study. Greater understanding of brain functionality can lead to leaps in medical technology concerning brain disease and brain rescue implant techniques, but also leaps in engineering, concerning more refined Artificial Intelligence or even new non-von-Neumann computer architectures. As a result, SNNs are widely used in neuroscientific research to complement biological experiments.

In-vivo and in-vitro experiments are a traditional tool of neuroscientific research. They are powerful experimentation methods, but are also time-consuming and not always reliable. A number of factors can contaminate results like, for example, the influence of anesthesia in in-vivo experiments. What is more, most systemic phenomena require the monitoring of biological systems of very large scale and many such techniques do not allow for this kind of study. Computational neuroscientists use SNNs to circumvent such issues. By incorporating SNN models of varied complexity (which themselves are derived by biological experiments) they create predictive simulators that can test their scientific hypotheses and drive more targeted, thus more reliable and refined, biological experimentation [4].

A major challenge has to do with the sheer computational complexity that many SNN models include, compared to the older, simpler modeling classes. Even the less complex types of SNNs have significant demands as the studied neuronal network increases in size both in terms of computation and data transfer or storage. Traditional methods of computing, in which the common simulation tool-flows (such as MATLAB or specific neuro-modeling tools like NEURON or BRIAN) are executed, are not up to the task of simulating large-scale or very accurate neural networks within a reasonable timeframe for brain research, limiting the benefits that SNNs can provide. High Performance Computing (HPC) has been recently recognized as being able to provide a variety of solutions to cope with this limitation [5–10]. Unfortunately, the challenge of executing these simulation applications does not stop just at providing the necessary computational power.

In scientific applications, such as neuronal simulations, the model aspects have immense effect on simulation performance. The variety of options of viable SNN models used in studies is significant. Every type of model has scientific merit, depending on the subject under study, and models have significantly different characteristics when treated as computational workloads [9, 11]. Extra modeling features, like inter-connection of various densities between neurons (the modeling of which also varies according to the biological system that is under study) can break the embarrassingly parallel (data-flow compatible) nature that most neuron models have, significantly changing the behavior of the application.

In addition to this, there are also two distinct general types of simulations that are relevant in computational neuroscience. The first one has to do with highly accurate (biophysically accurate and even accurate to the molecular level) modeling of generally smaller sized networks that requires real-time or close to real-time performance. These kinds of experiments can be used with artificial real-time set-ups or brain-machine interfaces (BMI) and are closely related to brain rescue studies (TYPE I). The second type revolves around the simulation of large or very large-scale networks (in which accuracy often needs to be sacrificed). These experiments attempt to simulate network sizes and connection densities closely resembling their biological counterparts (TYPE II experiments) [8] [12]. This, in combination to the variety of models commonly used, makes for a field that includes applications that vary greatly in terms of workload, while also, depending on the case, requiring high throughput, low latency or both. A single type of HPC fabric, either software or hardware based cannot cover all possible use cases with optimal efficiency.

A better approach is to provide scientists with an acceleration platform that has the ability to adjust – on the fly – to the aforementioned variety of workload characteristics. A heterogeneous system that integrates multiple HPC technologies, instead of just one, would be able to provide this. In addition, a framework for a heterogeneous system using a common user interface for all integrated technologies can also provide the ability to dynamically select a different accelerator, depending on availability, cost and performance.

Such a hardware back-end must overcome additional challenges to be used in the field. It requires a front-end which should provide two very important features:

- An easy and commonly used interface through which neuroscientists can employ the platform, without the constant mediation of an engineer.
- A front-end that can reuse the vast amount of

models already present in the field.

Developing and executing experiments with SNN models is a very rigorous process since experimenting with the models presupposes their careful fitting to experimental data. The neuroscientist should be able to interface with the acceleration platform directly, which is not a standard practice today and incurs significant delays in the research process. Lastly, the ability to program the accelerator platform in commonly used coding languages and the portability of legend code, is essential for wide adoption of the HPC technologies by the community.

In this paper we propose a framework for a heterogeneous acceleration platform for computationally challenging neuroscientific simulations called BrainFrame. Using this system we demonstrate the effect of model characteristics on performance and thus making a concrete case on the significance of heterogeneity on an HPC system used in the field of computational neuroscience. To this end we use a state of the art extended-Hodgkin-Huxley neuron model of the inferior olive nucleus (InfOli) as a benchmark to evaluate the framework. We chose this model as a respective workload of biophysically meaningful neuron representations, as their efficient simulation poses a significant engineering challenge. We also evaluate using three different instances of the workload, each differentiated by the presence and complexity of the neuron interconnectivity modeling, leading to vastly different computational requirements, while still reflecting realistic neuroscientific-experiments. We propose a front-end for the framework based on the PyNN language [13]. PyNN is widely used in the computational neuroscience community and has direct integration with many other well-known neuron modeling frameworks, covering both features that such a front-end would require.

1.1. Neuron Modeling Background

The best choice of SNN model depends on the subject of the study a modeler needs to conduct [14]. There are three main categories of SNNs (although not the only ones): (A) *Integrate & Fire* models, (B) *Izhikevich* models, and (C) *Conductance(-based)* models.

The simplest version of SNNs are Integrate-and-Fire (I&F) models. They emulate the most basic operation of a biological neuron, which is the integration of spikes and firing using a threshold mechanism. From this most basic version, extensions are derived which add more features to the model’s behavior such as the Leaky I&F and quadratic I&F [15]. I&F models have extremely low computational demands but also very limited biological plausibility. They are, thus, useful for exploring large-scale network dynamics in relation

to the very basic features they can emulate. Izhikevich neurons [16] are a special type of models which – although featuring similar complexity to I&F models – emulate an impressive fraction of the biological-neuron behavior. This model type boasts the ability to emulate most input/output spiking activity found in the biological neuron. Although it treats the neuron as a black box, its flexibility permits to create very accurate high-level representations of large-scale, biological-neural-network behavior.

If, on the other hand, a researcher seeks to explore the electrochemical characteristics that produce the neuron’s response, a biophysically-meaningful neuron model is required, such as conductance-based models. They capture closely the electrochemical behavior that produces the neuron activity by modeling the various ion channels observed in biological neurons. The most prominent conductance-based model is the one originally presented by Hodgkin and Huxley (HH) in 1,952 [17]. HH models, and their variants, make heavy use of differential equations and are quite scalable, making the design of multi-compartmental models possible (the term “compartment” is used for the distinct parts of an accurate white-box neuron representation). The computational complexity of conductance-based models is orders-of-magnitude higher than that of the aforementioned types [14], posing a significant challenge for their efficient simulation.

2. Methods

2.1. The Inferior Olive

The inferior olive nucleus forms an intricate part of the olivocerebellar system, which is one of the most dense brain regions and plays an important role in sensorimotor control. Activity in the inferior olive probably only directly triggers movements, when it is synchronized among multiple neurons [18, 19]. In addition, the olivary neurons can provide rhythm and coordination signals for motor functions [20]. It is considered to be imperative for the instinctive learning and smooth completion of motor actions [21]. The olive provides one of the two main inputs to the cerebellum through the so called climbing fibers.

The inferior olive neurons are also heavily interconnected to one another through electrical connections called gap junctions (GJs), which differ from typical synapses since they are purely electrical. The gap junctions facilitate the synchronization behavior between the olivary neurons and, subsequently, influence the synchronization and learning properties of the entire olivocerebellar system [20].

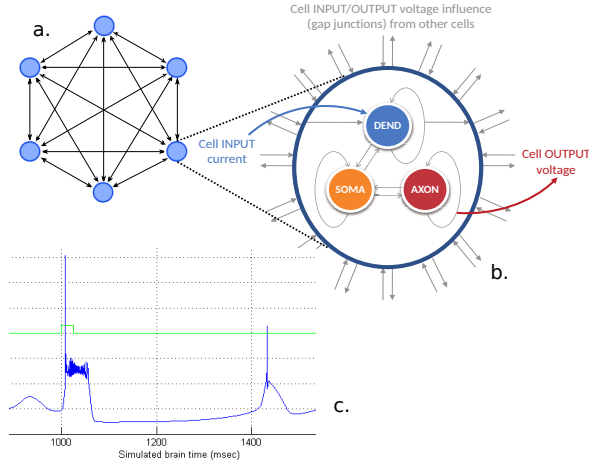


Figure 1. Graphical representation of the inferior-olivary network model. a) 8-neuron network b) single-neuron model in detail c) sample axon response.

2.2. The InfOli Workload

In this work a detailed inferior olive (InfOli for short) model is considered, which was originally developed by De Gruijl et al. [4]. It is an extended-HH (eHH) model representation of the inferior-olive cell. It implements a neuron with three distinct compartments, the dendrite, the soma and the axon. Within the dendrite, the model also includes gap junctions (thus characterized as “extended”). The dendrites represent the cell input stage, the soma is the cell part wherein most of the neural processing takes place, and the axon represents the cell output stage towards the climbing fibers (Figure 1b). The GJs are associated with important aspects of cell behavior as they are not just simple connections; rather, they involve significant and intricate electrical processes, which is reflected in their software implementation.

Every compartment includes a number of state parameters denoting its electrochemical state and the *neuron state* as a whole. The neuron states are updated at each simulation step; every new state update is based upon: The neuron state of the previous simulation step of the executed neuron, the previous dendritic states coming from the GJ connectivity and the externally evoked input to the network, representing the input coming from the rest of the cerebellar circuit.

The three compartments and GJs are evaluated/updated concurrently at each simulation step. The model is calibrated with a simulation time step of $\delta = 50 \mu\text{sec}$. This simulation step also defines *real-time performance*. Every simulation step for the entirety of the network must be completed within $50 \mu\text{sec}$ for the execution to be considered real-time.

Table 1. Neuron computational requirements per simulation step.

Computation	FP Operations per neuron
Gap Junction	12 per connection
Cell Compartment	859
I/O and storage	FP Operations per neuron
Neuron States	19
Evoked Input	1
Connectivity Vector	1 per connection
Neuron Conductances	20
Axon Output	1 (Axon Voltage)
Neuron Computation Task	% of FP ops for 96 cells
Compartmental Computations	43
Gap Junctions	57

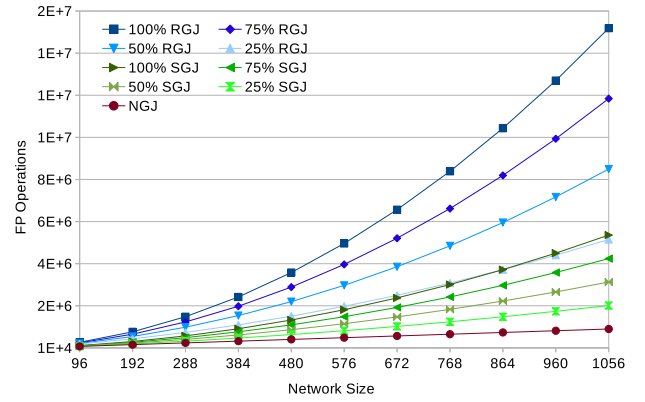


Figure 2. Floating-point operations needed per simulation step of the InfOli model for each use case and for different connectivity densities.

Figure 1a depicts a representation of the InfOli network model. The GJs are part of the dendritic compartment, thus the compartment receives the extra input coming from the inter-neuron connection. The network model works in lock-step, computing discrete output axon values (with a $50 \mu\text{sec}$ time step) which, when aggregated in time, recreate the output response of the axon (Figure 1c). The InfOli network must be synchronized in order to guarantee the correct exchange of previous dendritic data within a step. Thus, the execution can only be parallelized in space (simultaneous execution of neurons within a step), but not in time (parallelization of simulation steps). The cells even when not actively spiking present an oscillatory behavior, thus affecting network synchronization. As a result, event driven execution of the network model is not an option.

By profiling the application using a operation and memory access profiler [22], it is revealed that the GJs have great impact on the total model complexity. As seen in Table 1, the total number of floating-point

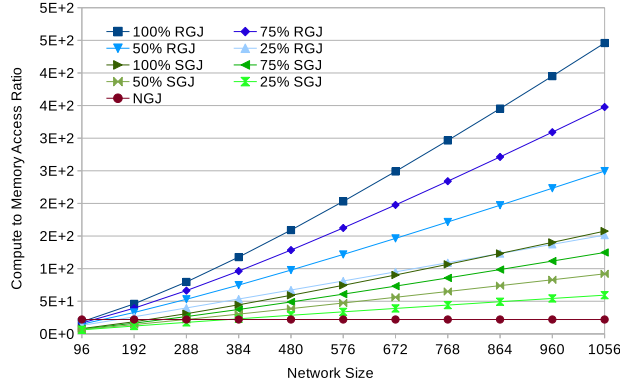


Figure 3. Compute to Memory Access Ratio per simulation step of the InfOli model for each use case and for different connectivity densities.

(FP) operations needed for simulating a single step of a single cell including a single GJ are 871 \ddagger . In an N -cell network, assuming that each neuron maintains a constant number of connections C to neighboring cells, the overall GJ computation cost exhibits linear complexity. For many complex experiments, it is not the number of connections C but, rather, the *connectivity density* that is indicative of neuron interconnectivity. That is, the *average percentage of the total neuron inventory to which neuron cells are connected* (measured in %), whereby the complexity becomes $\mathcal{O}_{gj}(N^2)$. This makes GJ computations the dominating factor, as they break the dataflow nature of the application and dominate computational demands. This is true even for small-scale networks. As an example, for a 96-cell, all-to-all connected network (Table 1) the GJs comprise almost 60% of the overall computations.

2.3. Application Use Cases

For our analysis, we use three use cases used in [11], which are representative of the memory and computational requirements of the InfOli workload. All of the use cases are realistic instances of the InfOli application and have neuroscientific merit. They can also be considered as plausible instances of multi-compartmental modeling using HH models with various cases of neuron connectivity modeling.

The application allows for the connectivity of the InfOli network to be programmable by the user before the simulation is deployed. The network connectivity (when present) is defined by an $N \times N$ *connectivity matrix* (where N is the network size) of FP weights signifying the weight of each connection. The weight value is used in the GJ computations to calculate the

\ddagger Table numbers have been updated to amend a profiling mistake reported in previous work [11].

connection impact on the neuron. The three use cases are focused around the biological complexity of the GJs:

- (i) **InfOli with Realistic Gap Junctions (RGJ)** – InfOli cells modeled with (biophysically) realistic GJ interconnectivity as presented in [4]. The highest amount of detail is included in the GJ modeling.
- (ii) **InfOli with Simplified Gap Junctions (SGJ)** – InfOli cells modeled with GJs replaced by simplified, passive connections. This constitutes a simpler connectivity in comparison to the previous use case.
- (iii) **InfOli with No Gap Junctions (NGJ)** – InfOli cells modeled without accounting for GJs and without any interconnectivity implementations. This is the simplest use case, whereby the neurons are modeled as separate computational islands.

In Figure 2, we see the amount of FP operations, based on the aforementioned profiling of InfOli application. The FP operations are counted for each of the aforementioned use cases for different connectivity densities. From the same profiling we can derive the compute (in FLOPS) to memory (in single-FP memory accesses) ratio for the application, that reveals whether each use case is computation- or memory-bound (Figure 3).

2.3.1. InfOli with Realistic Gap Junctions (RGJ)

This use case represents a fully featured version of the InfOli application. The complex Gap Junction dominates the computation in this use case. GJs here are implemented as a very specific representation of the biological nucleus (Algorithm 1). Each cell accumulates the influence of each GJ it integrates by subtracting its own dendritic voltage (`prevVdend`) from the dendritic voltage of the interconnected cell (`neighVdend[i]`). It, then, accumulates the resulting voltage influence on the `Ic` variable, factoring GJ-connection weight (`C[i]`).

The compute-to-memory ratio suggests also that this use case is strongly computation-bound for all connectivity cases: the computations increase at a much faster pace than the memory access requirements with increasing problem sizes.

Algorithm 1 Example of RGJ implementation in C

```

1: for i=0; i<InfOli.N.INPUT; i++ do
2:   V = prevVdend - neighVdend[i];
3:   f = 0.8*V*exp(-1 * V * V/100) + 0.2;
4:   Ic = Ic + (C[i] * f * V);
5: end for
6: return Ic;
```

2.3.2. InfOli with Simplified Gap Junctions (SGJ)

The level of detail as in the RGJ case is useful for many modeling experiments but is also an overkill in many other cases that more simple rudimentary connection are involved (like simple synapses that accumulate inputs). Lighter workloads are represented by the SGJ case. We assume a use case of the InfOli application that simplifies the connection between neurons to a few simple input accumulators. The accumulation is parameterized using the weight that is assigned to each connection between two neurons, thus the connectivity information needs to be accessed the same way as is in the RGJ case. This use case has significantly lower processing requirements. Even though increasing the network size leads to similar scaling trends as in the RGJ case, the actual FP operations are reduced by about one order of magnitude compared to the previous use case (Figure 2). Yet, the connectivity feature still breaks the data-flow nature of the main neuron modeling. A similar trend as before is seen also in the compute-to-memory ratio, since the computation still increases at a faster pace than the memory requirements.

2.3.3. InfOli with No Gap Junctions (NGJ) This is the case where the application becomes purely data flow and can achieve the greatest parallelism. The processing requirements scale almost linearly to the network size and, compared to the other use cases, fewer computations are needed, as shown in Figure 2. As we can see in Figure 3, although the NGJ use case shows that computation is still the most important aspect of the application, both computation and memory access scale linearly at a similar pace. Thus, the compute-to-memory aspect remains constant as the problem size increases.

2.4. HPC Fabrics and Implementation

Our heterogeneous platform incorporates three accelerator fabrics; a Maxeler *Maia* Data-Flow Engine (DFE) board [23], an Intel Xeon Phi 5110P [24] and a Maxwell-based Titan X GPU by NVidia [25] (Table 2). All these boards are PCIe-based which is how they communicate with the Host System. The three very different accelerators provide broad enough features to cover a variety of characteristics of our use case instances, discussed in the previous section.

The *Maia* DFE is a Maxeler HPC technology based on reconfigurable hardware. Its tool flow is designed and optimized to accommodate the acceleration of dataflow applications; that is, applications with the bulk of their implementation using purely raw computations with the absence (partially or totally) of branching execution or feedback paths. The Maxeler tools can exploit the nature of dataflow applications to

implement uniquely massive pipelines, maximizing the throughput and overall performance. The DFE boards also incorporate high-bandwidth, multichannel, highly parallel, customizable interface to the onboard DRAM memory resources (up to 96GBs) making it ideal for scientific applications. The DFE board used in our experimental setup is a 4th-generation *Maia*-DFE board implemented using an Altera Stratix V 5SGSD8 chip.

The Xeon Phi is an Many Integrated Core (MIC) architecture co-processor which features 61 cores, each capable of supporting up to 4 instruction streams. The generation of Phi cards used in this work, named Knight's Corner, are programmed using well-known programming tools such as OpenMP and OpenCL. However, and in contrast to GPU mentality, the Phi can also be thought of as an accelerator that can act as a stand-alone processor and even features its own Operating System. This is expected to increase memory consistency and cache coherency delays.

GPGPUs have also been prominent on the HPC and the scientific-computing domain specifically. The Titan X includes 3,072 CUDA microcores, which are used to parallelize computation execution, and 12 GB of on-board RAM. GPU implementations also benefit from the generally good adoption of the NVidia CUDA library open environment that allows porting of applications with similar ease to the Phi OpenMP and OpenCL frameworks. GPUs also come at a relatively lower cost than the other two accelerator types. However, as opposed to the the Xeon Phi, a GPU cannot act as its own host increasing communication delays between host and accelerator during execution.

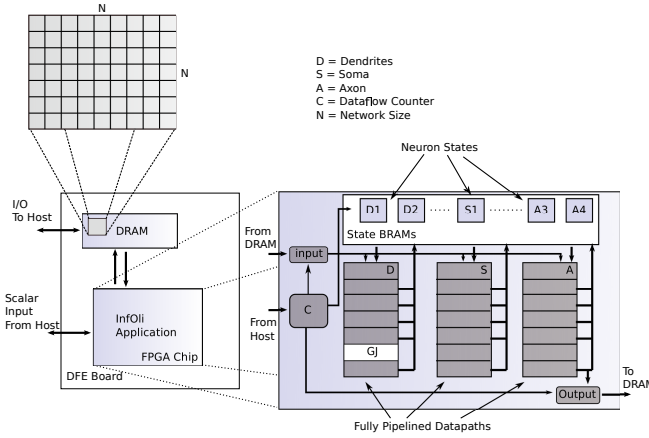
Lastly, it must be noted that BrainFrame is to be used in scientific research that is very dynamic and fast-paced. The goal is not to over-optimize the accelerator implementations, but keeping a balance between the programming effort and optimization, resulting to shorter development times. In realistic research scenarios the development time of the support of such a system should not delay the scientific process.

2.5. Infoli on the *Maia* DFE

The DFE implementation of the InfOli application can be seen in Figure 4 and is a more advanced version of the work done in [26]. Added features include the addition of programmable connectivity and programmable neuron state by the user between experiments runs without the need to re-synthesize the design. The design implements 3 pipelines on the DFE hardware to accelerate the application, one for each part of a neuron (Dendrite, Soma, Axon), executing the respective computations. The state parameters for each neuron are stored on separate BRAM blocks for fast read/update of the network state, as they are the data that are most used throughout the experiment

Table 2. Acceleration fabric specifications

Specification	Maxeler Maia DFE	Xeon Phi 5110P	NVidia Titan X
On-Board DRAM	48 Gb	8Gb	12 Gb
RAM bandwidth	76.8 Gb/s	320 Gb/s	336.5 Gb/s
Memory streams/channels	15	16	-
On-chip memory	6 Mb (FPGA BRAMs)	30 Mb (L2 cache)	3 Mb (L2 cache)
Number of chip cores	n/a	61	3072 CUDA Cores
Chip frequency	Depends on implemented design	1.053 GHz	1 GHz
Instructions set	n/a	64 bit	32 bit
Power consumption (TDP)	140 W	225 W	250 W

**Figure 4.** DFE implementation of the InfOli application.

execution. Since every new neuron state is dependent only on the network state of the previous simulation step, only one copy of each neuron state is required at any point in time. The input stream to the DFE kernel originates in the on-board DRAM and represents the evoked (external) inputs, used in the dendritic computations comprising the network input. The initialization data are also streamed in from the on-board memory only once at the start of execution. The size of the connectivity matrix makes it impossible to save on the on-chip memory. It is, thus, placed on the on-board RAM and streamed in batches dictated by the computations. The kernel output is streamed back to the on-board memory and – at the same time – is updated in the (on-chip) BRAM blocks of the DFE.

The program flow is tracked using hardware counters monitoring GJ loop iterations (except for NJG case), the neurons executed and the number of simulation steps concluded. The data flows through the DFE pipelines with each kernel execution step (or *tick*) consuming the respective input or producing the respective output and new state at the correct execution points according to the hardware counters. DFE execution naturally pipelines the

execution of different neurons within one simulation step. Simulation steps are not themselves directly parallelizable, as every neuron must have the previous state of all other neurons ready for its GJ computations (either RGJ or SGJ) before a new step begins. The DFE pipeline is, thus, flushed before a new simulation step begins execution. This dependency is alleviated when on the NGJ case. The GJ calculations is a loop that requires to finish before the rest of the dendrite compartment state is calculated. The rest of the dendrite pipeline does not produce valid data for the operation ticks that the GJ influence is being calculated. This delay is somewhat amortized by using hardware loop unrolling on the GJ calculations, but only to the point that the available chip area allows it. Additionally, in use cases where programmable connectivity is included, the ticks for the evaluation and execution of a GJ connection are always spent regardless of whether a connection actually exists or not. Thus, this implementation cannot benefit from a smaller connectivity density in terms of performance. On the other hand, since one synthesized design can account for all possible connectivity scenarios, the DFE implementation can guarantee predictable performance.

2.6. Infoli on the Xeon Phi

The InfOli application on the Intel Xeon Phi co-processor, depicted in Figure 5, is based on a shared-memory implementation, which is a more typical, software-based solution for HPC workloads. The application uses the OpenMP library to spawn threads, which can work in parallel. As the Xeon Phi 5110P uses one core to handle OS-related tasks and each core features multithreading technology that can service up to 4 instruction streams simultaneously, the InfOli application on the Xeon Phi uses up to $60 \times 4 = 240$ OpenMP threads. Each thread is programmed to handle a part of the neuronal network (sub-network), which is partitioned as uniformly as possible to prevent workload imbalances.

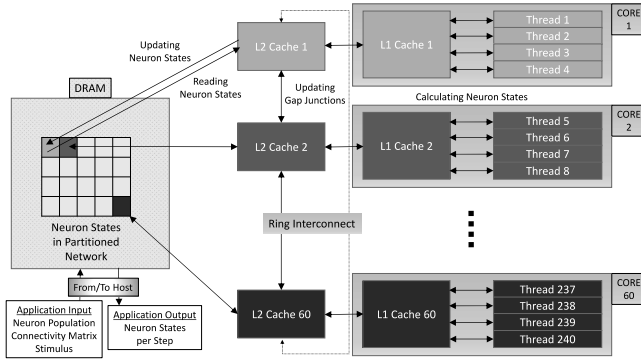


Figure 5. Phi implementation of the InfOli application

In each simulation step, the OpenMP thread is charged with computing its sub-network’s state. This process is further broken down into two tasks. Initially, the sub-network needs updated information on the rest of the network, specifically the voltage levels of dendritic membrane from other neurons in connection with this sub-network. Thus, the OpenMP thread accesses memory space shared by all threads in order to collect data from other neurons, with the purpose of re-evaluating the state of its sub-network’s GJs. In this task, shared-memory accessing can cause stalls in thread operations due to issues such as memory contention.

Upon completion of its first task, the OpenMP thread updates the compartmental states of each neuron in the sub-network. Each of the neuron’s three compartments is re-calculated (dendrite, soma and axon). The dendritic compartment specifically uses the updated GJ states evaluated in the previous task in order to assess the incoming current from connected neurons. This particular process demands an amount of operations that increases significantly with neuron population in the case of densely connected networks, as we would expect with the increasing computational demands of Gap Junctions.

After performing its two tasks for the entirety of its sub-network, the OpenMP thread begins the process anew for the next simulation step, until there are none left. Under this paradigm, the threads operate constantly within the “timeframe” of the same simulation step. They sync before the execution of a new simulation step, so that stale data from previous simulation steps cannot be exchanged during GJ computation. This behaviour is enforced due to the stiffness of the eHH model equations, which can be thrown off-balance even by the minute changes in data within a single time step. Under a more relaxed model, some staleness in data exchange would be more tolerable and the user would be able perform thread-syncing less frequently in order to trade precision for

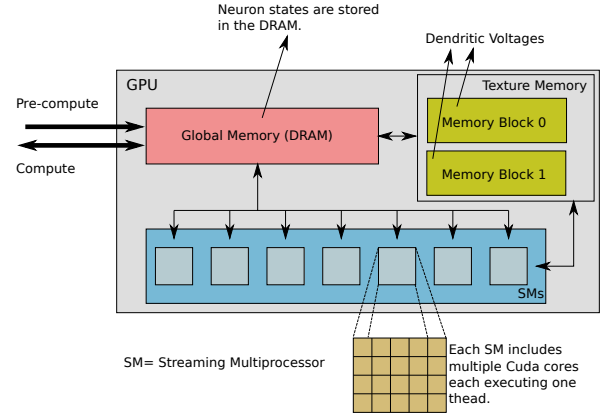


Figure 6. GPU implementation of the InfOli application. Pre-compute and Compute operations are issued by the host.

execution speed. Furthermore, it should be noted that the implementation described assumes that the entire network is large enough so that it can be partitioned in 240 parts. When dealing with smaller networks, the implementation utilizes less than the maximum amount of the platform’s assets, since it is designed to require at least one neuron for each OpenMP thread to operate on.

2.7. Infoli on the Titan X GPU

In Figure 6 we can see the Infoli implementation on the GPU. The execution flow includes two stages, a pre-compute and a compute stage.

In the pre-compute stage, the host initializes the neuron states and the external input currents for the entire simulation duration. It allocates global memory on the device to store the present neuron states, next neuron states and the external input currents. At the end of this stage, the host copies the required data for simulation onto the GPU. The current (in relation to the simulation step) dendritic voltage of cells (which is part of the neuron state) are accessed frequently as they are used to determine the GJ influence. To reduce memory latency, they are bound to the GPU texture memory. Texture memory is a cached memory on the GPU used to reduce memory latencies when the application has specific memory access patterns. Writes to texture memory, during the compute stage, are conducted only after all computations of a simulation step have finished. It must be also noted that after the pre-compute stage, no data is transferred from the host to the GPU as the GPU contains all the necessary information for the simulation.

During the compute stage, the neuron calculations are conducted and the new states are persistently stored throughout the simulation duration. To

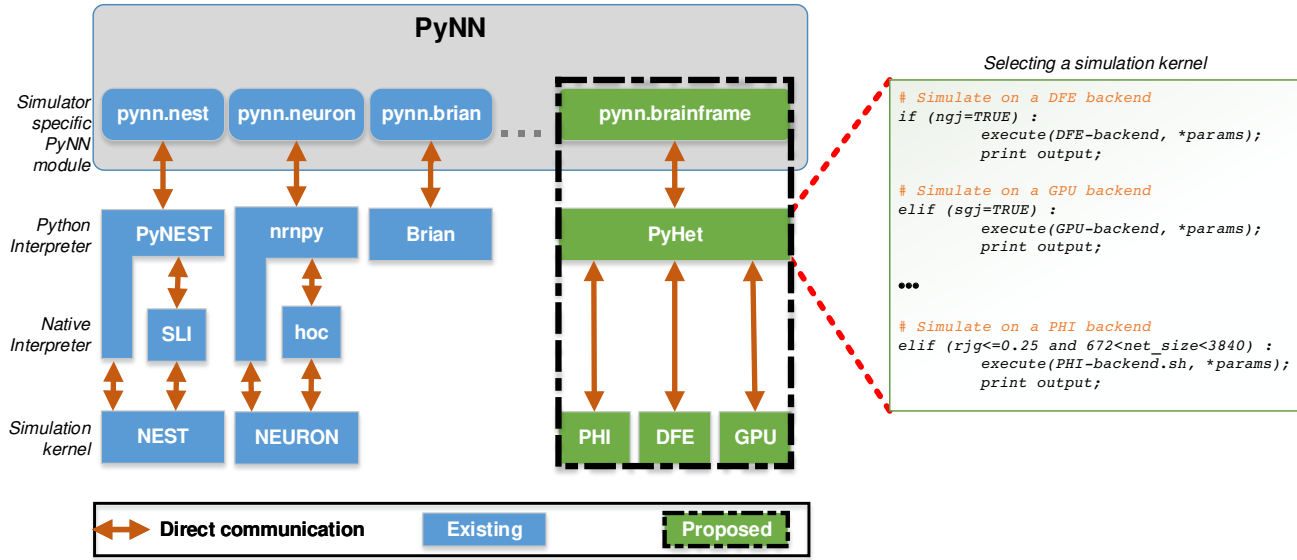


Figure 7. PyNN architecture and the proposed BrainFrame framework.

compute the new states for a single simulation step, the host launches a CUDA kernel on the device. Before simulation, the kernel is configured for a particular use case (RGJ, SGJ or NGJ) and interneuron connectivity scheme (if applicable). The kernel is executed by a 2-dimensional grid of CUDA threads on the device. Threads are executed in parallel by the CUDA micro-cores of the GPU. Every InfOli cell of the model is mapped to a corresponding thread that calculates the states of the neuron. On completion of the kernel, the host receives the calculated result of the simulation step from the device. The host uses two operation streams to issue the kernel execution and data transfer operations to the GPU. A kernel in one stream is launched only when the kernel in the other stream has completed. Thus, when one stream is computing the currently executing simulation step, the other stream is performing the necessary data transfers to the host from the GPU. Since the texture memory is updated only after the kernel completes execution, data coherency is maintained. Thus, computation of the current neuron states and data transfer of the previously computed states overlap, hiding Host-to-GPU transfer delays.

2.8. BrainFrame & the PyNN Front-End

PyNN is a Python package that facilitates the interchangeability and the study of different simulation environments within the computational neuroscience community [13]. It allows for simulator-independent specification of neuronal-network models and already supports many popular simulators like NEURON, NEST, PCSIM, Brian etc.

The PyNN API supports modeling at multiple levels of abstraction, both at the neuron level and the network level. It provides a library of standard neuron, synapse and synaptic-plasticity models and a set of commonly-used connectivity algorithms while also supporting custom user-defined connectivity in a simulator-independent fashion.

We integrated the three accelerators as backends on the BrainFrame system using PyNN as a front-end. The PyNN integration provides the neuroscientific community with easy access on the accelerators without the constant mediation by the acceleration engineer while also providing an interface for the already established models to be used with the acceleration back-end. These characteristics of PyNN can have decisive impact on the adoption of BrainFrame by the community.

As a proof of concept for the front-end of the BrainFrame platform, we have integrated the InfOli model in PyNN's standard models. Following the PyNN paradigm, the user initially selects the simulator, in our case our BrainFrame simulator, and then proceeds to select the neuron model, in our case the Inferior-Olive model. A population of neurons using the chosen model is then generated, determining the inter-neuron connectivity type and, finally, a projection of the specified neuronal network is created.

The main difference between the proposed PyNN-backend substrate and the typical simulator backends within the PyNN environment, is an additional selection step. In this step a decision about which of the three candidate acceleration fabrics will be used for a specific experiment is taken, based on the available hardware and the characteristics of the

simulated neural network.

An abstract view of the architecture of the PyNN Brainframe module is shown in Figure 7. In order for the simulator kernels to communicate with the PyNN frontend, an intermediate BrainFrame-specific PyNN module (`pynn.brainframe`) is required that implements and extends common methods and objects like the neuron models, synapse models and projection methods and objects. In the case of the proposed BrainFrame module, we implemented objects and methods for: i) initialization of the simulator, ii) the description of the neuronal network in PyNN, and iii) for controlling the simulation execution. In some cases an additional interpreter module is needed to translate these Python objects and parameters to each simulator’s native parameters and language. For our system we developed the PyHet – the BrainFrame-specific Python interpreter – which serves the aforementioned role and also implements the accelerator selection.

3. Results

In this section we present a thorough performance analysis of our heterogeneous BrainFrame platform. The goal is to evaluate the platform and give a clear view on how each accelerator performs when running the various instances of the use cases defined previously, validating the applicability of a heterogeneous HPC method for computational neuroscience. The performance analysis is also used as a guide for the back-end selection algorithm.

To validate the correct functionality of the implementations, we use a simple experiment that recreates a typical response that is found in the inferior-olive network (axon response). In this experiment each cell produces a so-called complex spike, seen in Figure 1c, from all simulated cells. 6 seconds of brain time is simulated, that translates to 120,000 simulation steps. The complex spike is produced by applying a small pulse as input to all InfOli cells at the same point after program onset for about 500 simulation steps (or 25 ms, in brain time). Despite being rudimentary, this experiment is easy to validate, provided all neurons are initialized with the same state, and also gives a good indication whether synchronization between neurons is correct, validating the interconnectivity between cells (when present).

As mentioned in the introduction, there are two distinct tracks that can be followed in conducting neuroscientific experiments, both covered in this evaluation. We perform one batch of measurements ranging from 96 to 960 neurons (representing small-scale/real-time TYPE-I experiments) and a second batch ranging from 960 to 7,680 neurons (representing

larger scale TYPE II experiments). We consider (consulting our neuroscience peers) the minimum meaningful network size for experiments to be around 100 neurons, thus our measurements for TYPE I experiments begin at 96 neurons. The evaluation is focused around single device performance thus the network size cap in the evaluation is defined by the smallest maximum network that is supported between the three accelerator fabrics (in the current case 7,680 that is the maximum supported network on the DFE fabric).

3.1. Performance Evaluation

All performance measurements concerning the Xeon Phi have been carried out with Intel’s profiling and analysis tool Vtune Amplifier XE 2015. Timing measurements on the Maia DFE were taken measuring the kernel time within the host code using timestamps before and after the kernel call. The CPU host code is blocking, thus, only the DFE kernel is active during the measurement. The time includes the kernel execution (processing and DRAM data-exchange delay) and the activation delay of the FPGA device. This activation takes about 1 ms, which is negligible compared to the overall execution time that takes several seconds to several minutes in our test experiment. GPU kernel time measurements were taken using the CUDA event libraries.

Starting with the analysis for TYPE I experimentation, in Figure 8 we can see the simulation step-execution time for the most demanding use case, that of the RGJ with 100% connectivity density. Even though not the most common case, a platform requires to support such high interconnectivity densities for certain TYPE I experiments. Here, we can see that the DFE has the best performance for all our network sizes. The Xeon Phi follows closely although still kept back due to the local memory delays and the less efficient use of its parallel threads. These network sizes are not large enough to provide sufficient parallelism for the Phi threads to be fully utilized. The GPU, on the other hand, has difficulties to cope with the computational intensity of the gap junctions, which involve mostly division and exponent FP calculations. Since each cuda thread executes one neuron it cannot exploit any potential parallelism in the GJ calculation. This, alongside the fact that the cuda threads are underutilized with such network sizes, decisively affects performance.

The inefficiency of the Titan GPU X in performing the realistic GJ computations is clearly revealed in the SGJ case (Figure 9). In this use case, that the most demanding GJ calculations are dropped, the GPU presents excellent scalability as the problem size increases, compared to the RGJ case. The Xeon

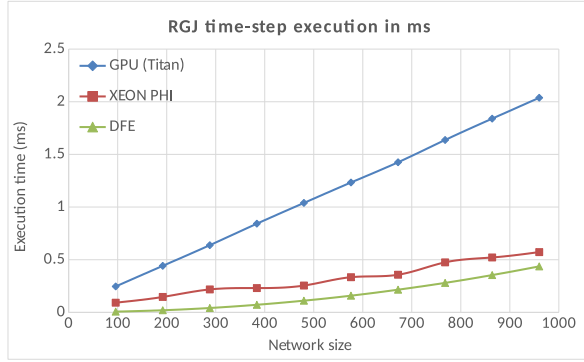


Figure 8. Execution time in ms for the RGJ case for 100% connectivity for TYPE I experiments.

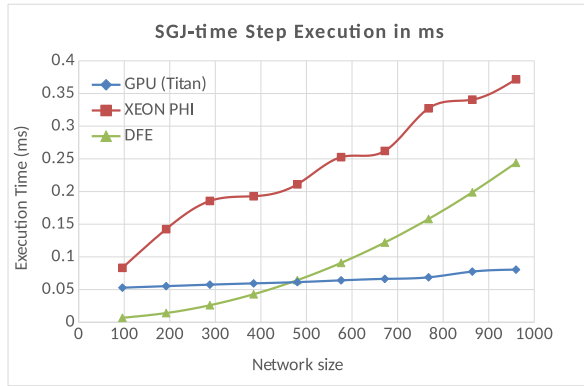


Figure 9. Execution time in ms for the SGJ case for 100% connectivity for TYPE I experiments.

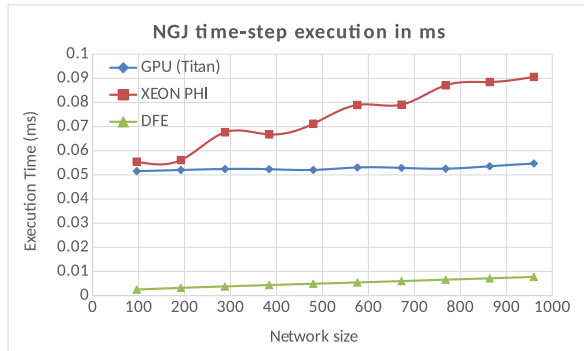


Figure 10. Execution time in ms for the NGJ case for TYPE I experiments.

Phi, on the other hand, still suffers from core-to-local-memory synchronization delays even though the actual calculations are much simpler now. The DFE, similarly to the RGJ case, needs to spent the same amount of operation ticks to evaluate the connection influence, even though it does enjoy gains in performance because of the simpler calculations (achieving higher operation frequencies, larger GJ computation parallelism and shorter pipelines). As a result, both accelerators show a similar scalability trend to the RGJ case. The

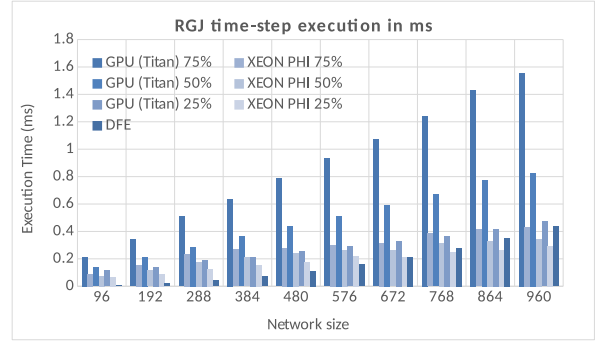


Figure 11. Execution time in ms for the RGJ case for lower than 100% connectivity densities for TYPE I experiments.

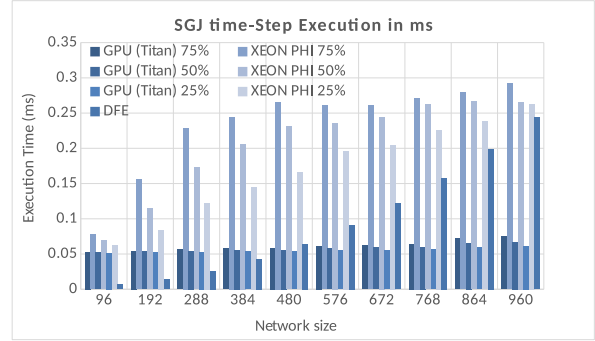


Figure 12. Execution time in ms for the SGJ case for lower than 100% connectivity densities for TYPE I experiments.

Table 3. Achievable network size (#cells) for each use case

Use case	Maia	Phi	Titan X
RGJ (100%)	310	-	-
RGJ (75%)	310	-	-
RGJ (50%)	310	-	-
RGJ (25%)	310	-	-
SGJ (100%)	400	-	-
SGJ (75%)	400	-	-
SGJ (50%)	400	-	96
SGJ (25%)	400	-	96
NGJ	7680	96	500

improvement in performance allows the Titan X GPU to perform better than the DFE for network sizes above 480 neurons.

Relevant for the evaluation and the design of the PyNn selection step is also the behavior of the three accelerators for less than 100% connectivity. Although not relevant for the DFE, as it cannot exploit performance benefits for less dense connectivities, smaller densities can influence the Phi and the GPU performance considerably. In Figure 11, we can see the simulation step performance for 25%, 50% and 75% connectivity densities, for the RGJ case. The

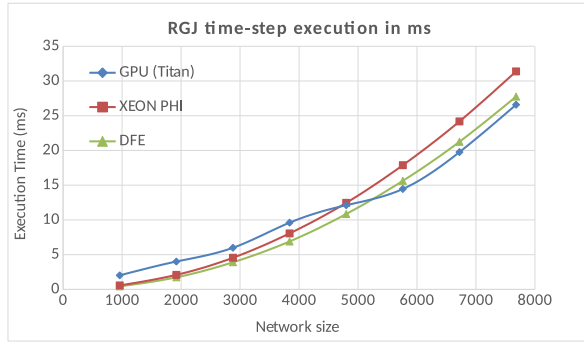


Figure 13. Execution time in ms for the RGJ (100% connectivity) case for TYPE II experiments.

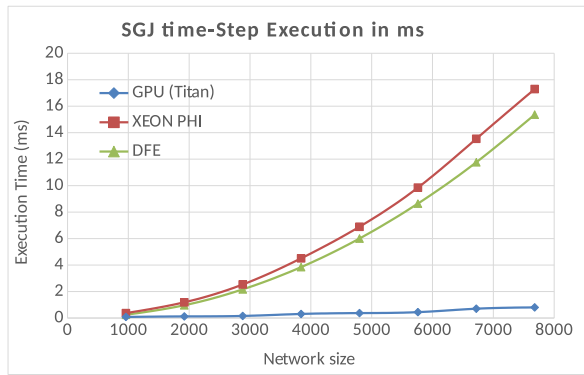


Figure 14. Execution time in ms for SGJ (100% connectivity) case for TYPE II experiments.

GPU delivers significant gains but the inefficient GJ execution still causes it to perform worse than DFE, even though the latter operates as in a 100% density simulation. The Xeon Phi, on the other hand, manages to have enough performance gains to become faster than the DFE for specific problem sizes and onwards. Specifically, above 960 neurons for 75% density and above 864 neurons and 672 neurons for 50% and 25% connectivity densities respectively. For the SGJ use case (Figure 12), we see similar trends as in the RGJ case. The end results are also the same as with the all-to-all SGJ connectivity runs. The GPU presents great scalability becoming the best option for network sizes higher than 480 neurons. The DFE remains the most beneficial option for networks smaller than 480.

For the NGJ case, for TYPE I experiments, the results point to the DFE as the uniformly best option. In the complete absence of the inter-neuron connectivity, the application becomes a purely dataflow task fully compatible for acceleration on a DFE, which is tailor-made for such cases, providing significant benefits over both the Phi and the GPU (Figure 10).

Lastly, for TYPE I experiments, what is important is the real-time capabilities of each platform. Table 3

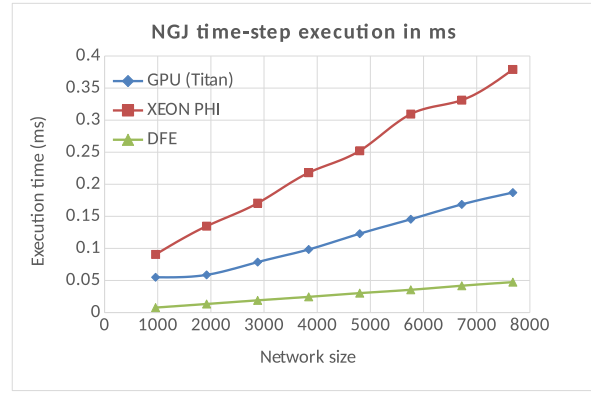


Figure 15. Execution time in ms for SGJ case on lower than 100% connectivity densities for TYPE II experiments.

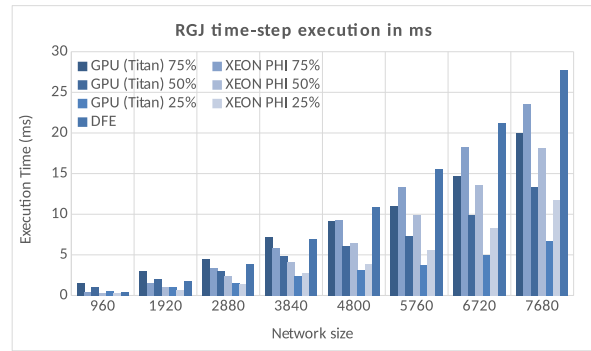


Figure 16. Execution time in ms for the RGJ for lower than 100% connectivity densities for TYPE II experiments.

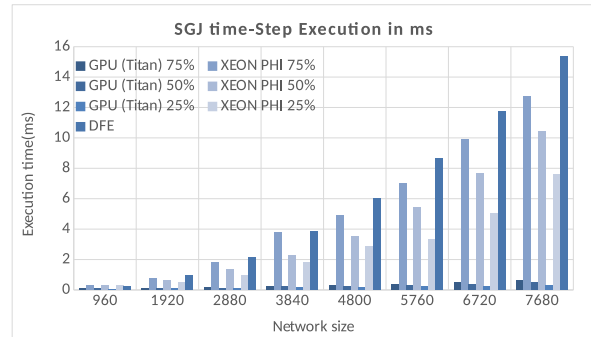


Figure 17. Execution time in ms for SGJ case on lower than 100% connectivity densities for TYPE II experiments.

presents the real-time achievable networks for each use case. The results show that, for real-time experimentation, the DFE accelerator is the most beneficial option for all cases. GPUs and Xeon Phi parallel threads tend to be underutilized at such small network sizes, even though most of the delays of using them are present. Thus the DFE, using a fine-grain pipelined kernel, can achieve greater benefits at the problems sizes that real-time execution is computationally achievable. It is interesting

to note that the DFE can even support real-time experimentation for TYPE II experiment on the NGJ case.

For TYPE-II experiments the trends for the RGJ case with 100% connectivity change significantly (Figure 13). Here, the massive explosion of the GJ computations begins to stress the parallelization capabilities of both the Phi and the DFE. The DFE’s efficient parallelization of the GJs relies mostly on the ability to unroll the GJ loop on the FPGA hardware, allowing for more iterations to finish per operation tick.

But the degree to which this unrolling can be accomplished is limited by available chip area. For network sizes above 1,000 neurons, the design is forced to reuse a lot of resources in time (as the unroll factor is limited), the dataflow paradigm breaks, and makes the application less scalable on the DFE. The Xeon Phi follows a similar trend, as the communication overhead between cores (which are organized with a moderately efficient ring topology [5]) causes the same effect on scalability. Even though the scalability of the two accelerators worsens when the problem size is increased, the GPU scalability is largely improved. The GPU is underutilized until all CUDA cores are used (3072) simultaneously, so for experiments over 3,000 neurons scalability is gradually improving. As a result, the GPU becomes the better performing solution for network sizes of 4800 neurons and above.

For lower connectivity densities, we see a similar trend, although the Xeon Phi scalability is slightly better because of the lower interconnectivity (Figure 16). Thus, the Phi retains the advantages it has for lower than 100% densities, compared to the DFE. Still, the effect of the inter-core communications is present allowing for the GPU to overtake the Phi for network sizes above 4800 neurons (for densities of 50% and 75%) and above 3840 neurons (for the 25% density). The same effect is also observed in the SGJ case for the DFE and Xeon Phi, although it is less pronounced. As a result, the GPU has no problem outperforming the other two devices types for any tested network size and connectivity density (Figures 14 and 17). Finally, in the NGJ case the situation is the same as with TYPE I. The dataflow nature of the application allows the DFE again here to present significantly better performance than the other two types (Figure 15).

3.2. Accelerator Selection Algorithm

The performance analysis discussed above can now be used to formulate a simple selection algorithm that will choose the accelerator based on the problem parameters, mainly connectivity detail (biophysically realistic: RGJ, simple: SGJ and not present: NGJ), density and network size. Figure 18 shows the selection

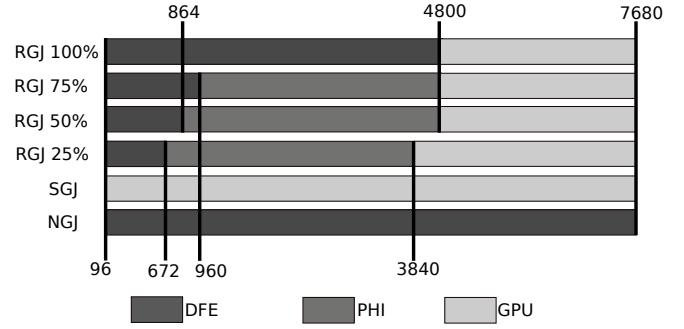


Figure 18. Representation of the selection based on which the pre-processing step in the proposed PyNN front-end chooses the most suitable accelerator.

for our use-case instances. The RGJ case selection, which presents the most complex case in terms of accelerator choice, shifts between all three options depending on the connectivity density. For the SGJ case, the GPU is always the accelerator of choice, while for the NGJ case the DFE is always selected. Lastly, if the experiment is flagged as a real-time experiment the algorithm chooses the DFE to accelerate the application, as it is the only clearly viable accelerator for real-time experiments.

As a simple example of how this selection can speed up experiments we can assume a scenario in which several batches of RGJ experiments need to be executed for various network sizes. Let us assume that each batch includes 5 experiments each with gradually decreasing connectivity density (100%-75%-50%-25%-0%) and that each experiment in a batch simulates 40 seconds of brain time. The time saving in this example by using the BrainFrame system compared to homogeneous systems that integrate *only a single* accelerator type can be seen on Table 4.

The BrainFrame can achieve significant benefits compared to the single fabric systems that can range up to 86% faster execution. On average, assuming the total runtime of all batches, the BrainFrame system can achieve 40% speed up compared to a pure DFE system, an 10.7% speed up to a pure GPU system and a 20.2% speed up compared to purely PHI-based system.

This selection can be easily extended/updated as new features and more generalized model libraries are added for acceleration (making the selection predictive for general cases) or as each acceleration technology is updated in the future.

4. Discussion

There are numerous related works that propose employing HPC solutions for the acceleration of SNNs. Such solutions include hardware-based solutions, like reconfigurable hardware, as well as software solutions

Table 4. Time saving in minutes with BrainFrame for the assumed experimental scenario compared to the homogeneous systems. In parenthesis the % speedups are shown.

Network Size	BrainFrame		
	vs DFE-only	vs Titan X-only	vs Phi-only
384	0.0 (0.0%)	24.2 (86.2%)	8.6 (68.7%)
960	3.2 (13.8%)	45.8 (69.5%)	3 (12.8%)
5760	1.9 (43.4%)	54.5(27.0%)	10.7(6.8%)
7680	591.7 (40%)	1.9 (0.2%)	246.6 (21.7%)
All Batches	707.7(40%)	126.4 (10.7%)	268.9 (20.2%)

using GPUs and less often many-core processors platforms, such as the Xeon Phi. Simpler modeling has found a good match on GPU-based systems, such as Izhikevich and I&F modeling [10, 27]. Higher biophysically meaningful modeling, like the extended-HH model, seems to be a much more difficult problem to solve with GPUs, especially for real-time experimentation [6].

The XEON Phi has also been used very successfully for bio-inspired neural networks, such as Convolutional Neural Networks for Deep Learning Systems [28]. On the other hand, similar difficulties to the GPUs in the acceleration of the complex HH models, are identified with Xeon Phi platforms even for less densely interconnected networks [5].

FPGA-based solutions have been especially prominent in accelerating neuron applications, with impressive results specifically for biophysically meaningful modeling and real-time performance for such networks [7, 8, 29]. It is also revealed in related works conducting performance analysis, that an FPGA’s potential benefit varies greatly between SNN types, even without taking into account connectivity modeling that can decisively change the workload characteristics [9].

Recently, we have also seen use of the DFE for accelerating computational neuroscience application. On purely dataflow neuromodeling applications, the DFE can have great benefits both in large scale networks but also in real-time network performance [30]. Even in the cases of HH neurons that include highly accurate interconnectivity modeling (breaking the pure dataflow nature), the DFEs can accomplish greater benefits than traditional FPGA acceleration [26].

These works, though, present just a one-off implementation of a specific application instance, on a specific acceleration platform and most also ignore the variety of synapse modeling and its influence on the applications. Biophysically accurate models of biological systems, such as the ones using the HH description, are comprised mostly of a set of computationally challenging differential equations often implementing an oscillatory behavior. If neurons

are simulated as independent computational islands (NGJ case), then dependencies between the equations do not arise, allowing divide-and-conquer, data-flow and event-driven acceleration strategies to be used very efficiently. The moment interconnectivity between oscillating neurons is modeled (like GJs, input integrators, STDP synapses etc), the cells become coupled oscillators. The embarrassingly parallel and data-flow nature of the application is then broken. All neuron states need to be completely updated at each simulation step to retain correct functionality. This requirement, in turn, enforces the use of cycle-accurate, transient simulators and forbids event-driven implementations. As a result, a single HPC fabric is unable to cover all the aforementioned requirements to support a complete study, as our analysis also reveals.

The above difficulties makes it obvious why the majority of the computational-neuroscience community has so far meticulously avoided employing HH models and multi-compartmental models with complex connections on large problem sizes using conventional computing machines. The eventual use of biophysically plausible neurons and connections on a larger scale is required to explain biological behavior. Even though the details of the most important systemic behaviors of the modeled systems must revolve around very specific characteristics of the networks, thus possible to be revealed by generally simpler representations, the computational neuroscientist cannot know beforehand which of the numerous dynamics revealed from the biological measurements (from which the models arise) can be safely abstracted. Studies seeking to reveal systemic behavior need to start with complex representations before they know enough to apply more simplified modeling.

Additionally, most related works seem to suffer from limited re-usability value due to their user interface. They ignore the challenge of the neuroscientific community adopting the proposed platform and very few propose solutions to that end. Beuler et al. [31] developed a graphical interface alongside their FPGA-based simulator. Although it does provide ease of use

in experiments, it is still confined to only one platform and only one application with limited flexibility to be the basis of a more widely adopted system. Weinstein et al. [32,33] took the approach of developing their own modeling language to interface to their acceleration library, the DYNAMO compiler. Besides the limitation of using only FPGAs as the back-end platform, the DYNAMO compiler is a technically complete solution. Unfortunately, it failed to achieve wide adoption by the scientific community as it requires learning a new language and, additionally, the non-trivial process of porting older established neuron models to the new coding paradigm.

The most promising solution, both in terms of usability and computational ability, was proposed by Cheung et al. [34] in NeuroFlow. In this work, the researchers integrated PyNN to their DFE-based hardware library. Neuroflow also provides a very complete library of IPs in the back-end, covering a great portion of possible applications. Yet, the system is still integrating a single acceleration platform. What is more, the performance and efficiency analysis is only presented for a single use case of a generally simpler model (Izhikevich) and with connectivity modeling of medium complexity (STDP) and relatively lower density (about 10%). The behavior and performance of the system for the rest of the supported features is not self-evident and should be significantly different, especially for accurate modeling such as the HH and with high connectivity densities, as shown by our performance analysis on the DFE platform. Furthermore, many of the performance benefits are accomplished using event-driven simulations (each neuron processes only when an event is happening in its input), that cannot always be employed as discussed earlier.

To the best of our knowledge no prior work has considered a heterogeneous acceleration system for coping with the variability of the applications in the field. Additionally, the PyNN integration provides a familiar interface to the neuroscientific community, thus making BrainFrame a complete solution for a node-level heterogeneous system. Even though BrainFrame is meant to be used in a single node system that integrates all three accelerator fabrics using the PCI-e, the way the framework is structure and implemented does not have to limit itself only in such a system. With minimal effort the BrainFrame paradigm could also be used on a multi-node environment with homogeneous nodes using any of the three HPC fabrics or even HPC solutions that integrate host and accelerators on-chip.

5. Conclusions

In this paper, we propose BrainFrame a heterogeneous acceleration platform to serve computational neuroscience studies in conducting the variety of experimentation, often required for the study of brain functionality. We focus our analysis on biophysically-accurate neuron modeling, as such modeling is essential for the understanding of the system properties of biological brain networks. In order for the system to cope with the inherent flexibility and variety of the field we present a proof-of-concept heterogeneous HPC system that integrates three HPC technologies already proven useful for brain simulations. The performance analysis of the system using use cases that take into account connectivity density and connectivity modeling complexity, reveals that all three fabrics are required to be integrated within a system to efficiently serve all possible experimentation cases. The platform is, thus, efficient for both TYPE I and TYPE II experiments and also provides real-time performance for meaningful network sizes.

Based on these observations, we have combined the three accelerators with a PyNN front-end and implemented a selection algorithm identifying the most suitable HPC accelerator, depended on the parameters of each desired experiment. Since all the accelerator use PCI-e slots to be integrated to the host system, great flexibility is also provided for the practical deployment of such systems, as the composition of hardware can be adjusted on a per-case basis depending on the availability of funds and hardware resources. Finally, the PyNN front-end creates a direct link of the simulation platform to a multitude of prior modeling works which is essential for wide adoption of the platform, while providing a clear roadmap for further development of our framework.

6. Acknowledgements

This work is partially supported by the European-Commission Horizon2020 Framework Programme Project Vineyard (Grant Agreement No 687628) and ERC-PoC-2014 project BrainFrame (SEP-210151915). We also like to thank the STFC Hartree Centre (UK) for providing the Maxeler and Xeon-Phi computational resources used in our experiments. We gratefully acknowledge the support of NVidia Corporation with the donation of the Titan X GPU used in this research and the continuous support provided by Maxeler Technologies throughout the research effort.

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